Past Presentations & Publications by Sau-Ching Wong

" CMOS Erasable Programmable Logic with Zero Standby Power "

Sau Wong, Hock So, Chuan Hung, Jung Ou

Presented at: 1986 IEEE International Solid-State Circuits Conference (ISSCC), Feb 19~21 1986, Anaheim, CA

Abstract: Programmable logic ICs with a complexity of up to 2000 gates will be reported. An input transition detector powers up the circuits and differential logic in the critical speed paths affords a 25ns delay.

10.1109/ISSCC.1986.1156900

" Novel Circuit Techniques for Zero-Power 25ns CMOS Erasable Programmable Logic Devices (EPLD's) "

S.C. Wong, H.C. So, C.Y. Hung, J.H. Ou

Published in: IEEE Journal of Solid-State Circuits: October, 1986 Volume: 21, No. 5 (pp 766~774)

Abstract: A family of CMOS erasable programmable logic devices (EPLDs) is described with emphasis on the state-of-the-art chip architecture and circuit design techniques. The main features of this family of EPLDs include zero standby power, high-speed operation, flip-flop reconfigurability, small chip size, and high reliability. A novel input-transition-detection circuit allows the chip to consume no power during standby and yet wakes the chip up with minimum delay. Basic architectural differences between EPLDs and EPROM are discussed that require extra design considerations to achieve an optimal speed path through the array. A direct-drive technique is used in the transistor-transistor logic buffer and flip-flop circuits to improve speed, layout area, and chip organization.

https://doi.org/10.1109/jssc.1986.1052605

“ A 5000-gate CMOS EPLD with Multiple Logic and Interconnect Arrays ”

Sau C. Wong, Hock C. So, Jung H. Ou, John Costello

Presented at: 1989 IEEE Custom Integrated Circuits Conference (CICC), May 15~18 1989, San Diego, CA

Abstract: A description is given of a CMOS electrically programmable logic device (EPLD) with over 220000 programmable elements organized into multiple logic array blocks (LABs) that communicate through a separate programmable interconnect array. Redundancy, for the first time ever in programmable logic devices, is implemented in both arrays to improve yield. Devices of different sizes can be easily constructed by varying the number of LABs and/or macrocells within one LAB. A 2X improvement in yield has been observed.

https://ieeexplore.ieee.org/document/5726166

“ Altera EP300 Design & Development Oral History Panel ”

Yiu-Fai Chan, Robert Frankovich, Robert Hartman, Clive McCarthy, Don (*Sau-Ching*) Wong

moderated by: Stephen Smith at Computer History Museum, Mountain View, CA (recorded on August 20, 2009)

Altera EP300 Design & Development Oral History Panel